AMENDMENTS TO THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A flip-flop circuit with embedded scan capabilities and having a master stage and a slave stage comprising:

a data input control stage that selectively controls a value on a data node that is coupled to the master stage and the slave stage; ~~and~~

a scan input control stage that selectively controls a value on a scan node that is coupled to the master stage[[,]];

a clock input control stage that generates a plurality of clock signals dependent on a clock input thereto~~provides delayed versions of the clock input and is coupled to the data input control stage and the scan input control stage~~,

wherein the plurality of clock signals are used to control the data input control stage, the scan input control stage, the master stage, and the slave stage, and

wherein one of the data node and the scan node is held constant when the other of the data node and the scan node is active.

2. (Original) The flip-flop circuit of claim 1, wherein the data input control stage inputs a data input signal and a scan enable signal, and wherein the data input control stage resides on one end of the flip-flop circuit.

3. (Previously Presented) The flip-flop circuit of claim 2, wherein the scan input control stage inputs a scan input signal and a scan enable signal, and wherein the scan input control stage resides on another end of the flip-flop circuit.

4. (Cancelled)

5. (Previously Presented) The flip-flop circuit of claim 1, wherein the scan node is active during a scan mode.

6. (Previously Presented) The flip-flop circuit of claim 5, wherein the data node is active during a normal mode.

7. (Original) The flip-flop circuit of claim 1, wherein the master stage passes a value to the slave stage based on the values of the scan node and the data node.

8. (Currently Amended) The flip-flop circuit of claim 1, wherein the ~~further comprising: a~~ clock input control stage ~~that~~ generates delayed and inverted clock signals to the data input control stage, the scan input control stage, the master stage, and the slave stage.

9. (Original) The flip-flop circuit of claim 8, wherein a data input signal selectively controls the value on the data node dependent upon the clock input control stage.

10. (Original) The flip-flop circuit of claim 8, wherein a scan input signal selectively controls the value on the scan node dependent upon the clock input control stage.

11. (Original) The flip-flop circuit of claim 8, wherein the master stage selectively passes a value to the slave stage dependent upon the data node, the scan node, and the clock input control stage.

12. (Original) The flip-flop circuit of claim 8, wherein the slave stage selectively controls an output of the flip-flop circuit dependent upon the data node and the clock input control stage.

13. (Currently Amended) A method for performing operations using a flip-flop with embedded scan capabilities and having a master stage and a slave stage, comprising:

selectively controlling a value on a data node dependent upon a data input control stage and a clock input control stage, wherein the data node is coupled to the master stage and the slave stage;

selectively controlling a value on a scan node dependent upon a scan input control stage and the clock input control stage, wherein the scan node is coupled to the master stage;

selectively controlling the slave stage dependent upon the master stage and the clock input control stage; ~~and~~

selectively generating an output of the flip-flop dependent upon the slave stage[[,]];

generating a plurality ~~delayed versions~~ of clock signals dependent on a ~~the~~ clock input thereto ~~to the data input control stage and the scan input control stage~~, and

using the plurality of clock signals to control the data input control stage, the scan input control stage, the master stage, and the slave stage,

wherein one of the data node and the scan node is held constant when the other of the data node and the scan node is active.

14. (Cancelled)

15. (Previously Presented) The method of claim 13, wherein the scan node is active during a scan mode.

16. (Cancelled)

17. (Previously Presented) The method of claim 13, wherein the data node is active during a normal mode.

18. (Currently Amended) The method of claim 13, further comprising:

inputting ~~a~~ the clock input ~~signal~~ to the clock input control stage; and

selectively generating delayed and inverted versions of the clock input ~~signal~~ there[[ ]]from.